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EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,291	TABRIZI, BEHNAM	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this c mmunication appears n the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4, 7 - 18, 20 - 22, 32, 35, 36, 40 - 45, 47 and 48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 7 - 18, 20 - 22, 32, 35, 36, 40 - 45, 47 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 23, 2003 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on October 23, 2003 has been received and entered in the case.

Claim Objections

3. Claim 35 is objected to because of the following informalities: "324" [sic: 32]. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 41, 45, 47 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 41, line 2, "the second conductive layer" lacks antecedent basis.

In claim 45, lines 5 and 6, "an electrically conductive material" lacks antecedent basis because there are more than one electrically conductive material in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 7 - 18, 20 - 22, 32, 35, 36, 40 - 45, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gramann et al. '151 in view of Mahulikar et al. '835.

Regarding claim 1, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- an electronic device package (a package in Fig. 1) formed from an integral silicon wafer (7) having a recess (8), the recess including a conductive region (12, at the bottom surface of the recess 8);
- a bare die electronic device (1) having a top, a bottom, sides, and a plurality of terminals (22 and 23), including a non-top terminal (22), the device being disposed in the recess and physically coupled to the package by a conductive bonding material

(AuSn solder), and wherein the non-top terminal is electrically coupled to the conductive region by the conductive bonding material; and

- a dielectric material (27) disposed.

Gramann et al. does not disclose a shape of the dielectric material to form a planar surface over the recess that is level with or higher than the top of the device. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a dielectric material (60) to form a planar surface over a recess (68) that is level with or higher than the top of a device (62). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the dielectric material as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 2, Gramann et al. discloses in e.g., Fig. 1 and column 5, lines 43 – 45 the conductive region (12, at the bottom surface of the recess 8) being formed by metallization.

Regarding claim 7, Gramann et al. does not disclose a plurality of metallized bumps in a plane. However, Mahulikar et al. teaches in e.g., Fig. 12 a plurality of metallized bumps (solder balls or 70) in a plane. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Gramann et al. by using the plurality of metallized bumps as taught by Mahulikar et al. The ordinary artisan would have been motivated to further modify Gramann et al. in the manner described above for at least the purpose of increasing the bond strength between the package and the external device (e.g., PCB). Furthermore, after modification of Gramann et al., the bumps are formed on the plain surface

(the surface of the elements 16 and 17) of the package of Gramann et al. Thus, Gramann et al. meets the following limitation "wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal".

Regarding claim 8, Gramann et al., as modified, discloses the package including a top and a bottom; and the bumps are located above the top of the package.

Regarding claim 9, Gramann et al. discloses in e.g., Fig. 1 the device (1) being a vertical device and the bottom of the device is coupled to the package in the recess (8).

Regarding claim 10, Gramann et al. discloses in e.g., Fig. 1 a second conductive region (13, at the bottom of the recess 8) coupled to a terminal (23) other than the non-top terminal (22).

Regarding claim 11, Gramann et al. discloses in e.g., Fig. 1 a plurality of contact (16 and 17) including at least a first contact (17) and a second contact (16), the first contact (17) being electrically coupled to the non-top terminal (22) and the second contact (16) being electrically coupled to a terminal (23) other than the non-top terminal.

Regarding claim 12, Gramann et al. discloses in e.g., Fig. 1 the plurality of contacts reside in the same plane.

Regarding claim 13, Gramann et al. does not disclose a second layer of dielectric completely covering the silicon wafer and the device except for the plurality of contacts. However, Mahulikar et al. teaches in e.g., Fig. 7 a second layer of dielectric (26) completely covering a substrate (52) and a device (54) except for the plurality of contacts (44). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Gramann et al. by using the second layer of dielectric to completely cover the silicon wafer and the device except for the plurality of contacts as taught by Mahulikar

et al. The ordinary artisan would have been motivated to further modify Gramann et al. in the manner described above for at least the purpose of protecting the die and the wafer.

Regarding claim 14, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- an electronic component package (a package in Fig. 1) formed from an integral silicon wafer (7) having a recess (8), the recess including a first conductive region (12, at the bottom surface of the recess 8); and
- a bare die electronic device (1) having a top, a bottom, sides, and a plurality of terminals (23 and 22), including a non-top terminal (22) and a top terminal (23), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), wherein the non-top terminal (22) is electrically coupled to the first conductive region (12, at the bottom surface of the recess 8) by the conductive bonding material, and the top terminal (23) is electrically coupled to a second conductive region (13 and 16); and
- a dielectric material (27) disposed in the recess.

Gramann et al. does not disclose a shape of the dielectric material to form over the recess. However, Mahulikar et al. teaches in e.g., Fig. 12 a shape of a dielectric material (60) to form over the recess (at the place of 60) such that at least a portion of a first and second conductive regions (the area on the base 62 where are connected to the wires 58) are essentially planar (the surface of 60). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the dielectric material as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify

Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 15, Gramann et al. does not disclose the second conductive region being a solder bump. However, Mahulikar et al. teaches in e.g., Fig. 12 a solder bumps (solder balls or 70) in a second conductive region (an area under the solder balls). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Gramann et al. by using the solder bumps as taught by Mahulikar et al. The ordinary artisan would have been motivated to further modify Gramann et al. in the manner described above for at least the purpose of increasing the bond strength between the package and the external device (e.g., PCB).

Regarding claim 16, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- an electronic component package (a package in Fig. 1) formed from an integral silicon wafer (7) having a recess (8), the recess including a first conductive region (12, at the bottom surface of the recess 8); and
- an electronic device (1) having a top, a bottom, sides, and a plurality of terminals (22 and 23), including a non-top terminal (22) located in a region other than the top of the device, the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), wherein the non-top terminal (22) is electrically coupled to the first conductive region (12, at the bottom surface of the recess 8) by the conductive bonding material; and
- a layer of insulation (27) disposed.

Gramann et al. does not disclose a shape of the layer of insulation to form a planar surface over the recess that is level with or higher than the top of the device. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a layer of insulation (60) to form a planar surface over a recess (68) that is level with or higher than the top of a device (62). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the layer of insulation as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 17, Gramann et al. discloses in e.g., Fig. 1 one of the terminals (23) of the device (1) being a top contact located at the top of the device; and the package (a package in Fig. 1) having a package top, wherein the package top also including a contact (17) coupled electrically via the conductive region to the non-top terminal (22).

Regarding claim 18, Gramann et al. discloses in e.g., Fig. 1 and column 5, lines 43 – 45 the conductive region (12, at the bottom surface of the recess 8) comprising a layer of metal; and the electronic device (1) resides within the recess (8) and the metal is electrically coupled to the non-top terminal (22) of the device (1).

Regarding claim 20, Gramann et al. discloses in e.g., Fig. 1 the metal of the conductive region (12, at the bottom surface of the recess 8) extending to a portion of the package top, the electronic component further comprising: a bottom contact (22) electrically coupled to the metal (17) on the package top.

Regarding claim 21, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- an electronic device (1) having a first terminal (23) and a second terminal (22), wherein a first dimension is defined therebetween;
- an electronic device package (a package in Fig. 1) having a first surface, the package formed from an integral silicon wafer (7) having a recess (8) on the first surface that has a depth that is substantially equal to the first dimension, the package further having a layer of metal (12) applied to the recess and to a portion of the first surface, wherein the electronic device resides within the recess and is physically coupled to the package by a conductive bonding material (AuSn solder), and the second terminal (22) is electrically coupled to the layer of metal (12) by the conductive bonding material (AuSn solder); and
- a layer of insulating (27).

Gramann et al. does not disclose a shape of the layer of insulation to form a planar surface over the recess that is level with or higher than the top of the device. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a layer of insulation (60) to form a planar surface over a recess (68) that is level with or higher than the top of a device (62). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the layer of insulation as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 22, Gramann et al. discloses in e.g., Fig. 1 a first contact (16) coupled to the first terminal (23); and a second contact (17) coupled to the metal (12) residing on the first surface of the package.

Regarding claim 32, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- a non-molded electronic component package (the package in Fig. 1) having a package top and formed from an integral silicon wafer (7) including a recess (8);
- a bare die electronic device (1) having a top, a bottom, sides, and a plurality of contacts (22 and 23), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), wherein at least one of the plurality of contacts (22) is electrically coupled by the conductive bonding material (AuSn solder) to a metallization layer (12); and
- a material (27) filling the recess (8) not occupied by the device (1) and conductive bonding material (AuSn solder).

Gramann et al. does not disclose a shape of the planarizing material filling to substantially create a level plane that includes the package top. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a planarizing material filling (60) to substantially create a level plane that includes the package top. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the layer of insulation as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 35, Gramann et al. discloses in e.g., Fig. 1 and column 5, lines 43 – 45 the metallization layer (12) couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

Regarding claim 36, Gramann et al. does not disclose a plurality of conductive bumps, each bump being disposed at a redistribution point. However, Mahulikar et al. teaches in e.g., Fig. 12 a plurality of conductive bumps (solder balls or 70), each bump being disposed at a redistribution point (at the area under the solder balls). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Gramann et al. by using the plurality of conductive bumps as taught by Mahulikar et al. The ordinary artisan would have been motivated to further modify Gramann et al. in the manner described above for at least the purpose of increasing the bond strength between the package and the external device (e.g., PCB).

Regarding claim 40, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- an electronic device package (the package in Fig. 1) including a silicon wafer (7) having a recess (8), the recess including a conductive region (12, at the bottom surface of the recess 8);
- a bare die electronic device (1) having a top, a bottom, sides, and a plurality of terminals (22 and 23), including a non-top terminal (22), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), and wherein the non-top terminal (22) is electrically coupled to the conductive region by the conductive bonding material (AuSn solder);

- a material (27) filling the recess (8) not occupied by the device (1) and conductive bonding material (AuSn solder); and
- a plurality of contacts (16 and 17) including at least a first contact (17) and a second contact (16), the first contact (17) being electrically coupled to the non-top terminal (22) and the second contact (16) being electrically coupled to a terminal (23) other than the non-top terminal, wherein the plurality of contacts reside in the level plane.

Gramann et al. does not disclose a shape of the planarizing material filling to substantially create a level plane that includes the package top. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a planarizing material filling (60) to substantially create a level plane that includes the package top. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the layer of insulation as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 41, Gramann et al. discloses in e.g., Fig. 1 and column 6, lines 40 – 41 the second conductive layer (13, at the bottom of the recess 8) being non-wire bonded.

Regarding claim 42, Gramann et al. discloses in e.g., Fig. 1 and column 6, lines 41 - 44 the layer (27) of insulation being a dielectric.

Regarding claim 43, Gramann et al., as modified, discloses the conductive bumps being spaced. Furthermore, the limitation "for electrically coupling with a pre-printed circuit board" is intended use language which does not differentiate the claimed apparatus over Gramann et al. and Mahulikar et al.

Regarding claim 44, Gramann et al. discloses in e.g., Fig. 1 the electronic component being a flip chip.

Regarding claim 45, Gramann et al. discloses in e.g., Fig. 1, column 5, lines 54 - 56 and column 5, line 64 - column 6, line 9 an electronic component comprising:

- a silicon wafer (7) having a recess (8);
- a bare die electronic device (1) having at least one contact (22), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), the at least one contact (22) electrically coupled by the conductive bonding material (AuSn solder) to an electrically conductive material (12),
- the electrically conductive material (AuSn solder) coupling the at least one contact (22) to an electrical input (17) of the electronic component, wherein the electrical coupling is achieved by non-wire bonding, and
- a dielectric material (27).

Gramann et al. does not disclose a shape of the dielectric material to form a planar surface over the recess that is level with or higher than the top of the device. However, Mahulikar et al. teaches in e.g., Fig. 9 a shape of a dielectric material (60) to form a planar surface over a recess (68) that is level with or higher than the top of a device (62). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Gramann et al. by using the shape of the dielectric material as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Gramann et al. in the manner

described above for at least the purpose of protecting the package and at least some of the terminal areas.

Regarding claim 47, Gramann et al. discloses in e.g., Fig. 1 and Fig. 12 the bare die electronic device (1) being covered by the dielectric material (27) and the electronic component is a flip chip.

Regarding claim 48, Gramann et al. discloses in e.g., Fig. 1 and column 5, line 64 - column 6, line 9 the silicon wafer (7) being an integral piece of silicon.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gramann et al. in view of Mahulikar et al. as applied to claim 1 above, and further in view of Yoshida et al. (JP 59-145537) or Oji et al. (JP 58-197857)

Gramann et al. in view of Mahulikar et al. discloses the claimed invention except the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. However, Yoshida et al. or Oji et al. discloses the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Frei et al. and Kolesar, Jr. by adding the conductive region as taught by Yoshida et al. or Oji et al. The ordinary artisan would have been motivated to further modify Frei et al. and Kolesar, Jr. in the manner described above for at least the purpose of increasing adhesive strength between the conductive region and the device.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 14, 16, 18, 21 and 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fillion et al., Anderson et al. Nakamura disclose a semiconductor device in the semiconductor wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
1/7/04 10:39:04 PM

BRADLEY BAUMEISTER
PRIMARY EXAMINER